WHAT IS CLAIMED IS:

1. A method for fabricating a trench capacitor, comprising:

forming a trench in a substrate;

forming a first capacitor dielectric layer on a surface of said trench;

forming a conducting layer inside said trench;

forming a second capacitor dielectric layer on a surface of said substrate and on said conducting layer, wherein said substrate around said first and second capacitor dielectric layers serves as a bottom electrode;

forming a protruding electrode on said substrate, said protruding electrode being on said substrate around said trench and covering a junction between said trench and said substrate; and

electrically connecting said protruding electrode and said conducting layer, said conducting layer and said protruding electrode being an upper electrode.

2. The trench capacitor of claim 1, wherein said step of electrically connecting said protruding electrode and said conducting layer further comprises:

forming an inner dielectric layer on said substrate to cover said protruding electrode;

forming a contact window opening in said inner dielectric layer to expose a portion of said protruding electrode and said conducting layer; and

forming a conducting structure in said contact window opening.

3. A method for fabricating a dynamic random access memory cell, comprising:

forming a trench in a substrate;

forming a first capacitor dielectric layer on the surface of said trench;

forming a conducting layer inside said trench;

forming a second capacitor dielectric layer on the surface of said substrate and on said conducting layer, wherein said substrate around said first and second capacitor dielectric layers serve as a bottom electrode;

forming a protruding electrode and a gate electrode on said substrate, said protruding electrode being on said substrate around said trench and covering a junction between said trench and said substrate;

forming a plurality of drain/source regions in said substrate beside two sides of said gate electrode; and

electrically connecting said protruding electrode and said conducting layer, and said conducting layer and said protruding electrode being an upper electrode.

4. The method of claim 3, wherein said step of electrically connecting said protruding electrode and said conducting layer further comprises:

forming an inner dielectric layer on said substrate to cover said protruding electrode;

forming a contact window opening in said inner dielectric layer to expose a portion of said protruding electrode and said conducting layer; and

forming a conducting structure in said contact window opening.

5. The method of claim 3, wherein after said step of forming said protruding electrode and said gate electrode, the method further comprises forming a plurality of spacers on sidewalls of said protruding electrode and said gate electrode.

6. The method of claim 3, wherein after said step of forming said plurality of drain/source regions, the method further comprises forming a self-aligned silicide on an exposed portion of said protruding electrode and said conducting layer.

7. A trench capacitor, comprising:

a substrate having a trench;

a conducting layer filling said trench and extending to said substrate around said trench; and

a capacitor dielectric layer between surfaces of said trench and said conducting layer and between said conducting layer and said substrate, said conducting layer being an upper electrode, said substrate around said capacitor dielectric layer being a bottom electrode.

8. The trench capacitor of claim 7, wherein said capacitor dielectric layer comprises:

a first portion between the surface of said trench and said conducting layer; and

a second portion between said conducting layer and said substrate.

9. The trench capacitor of claim 8, wherein a material of said first potion is the same as a material of said second portion.

10. The trench capacitor of claim 8, wherein a material of said first portion is different from a material of said second portion.

11. The trench capacitor of claim 7, wherein said capacitor dielectric layer is at least one of an oxide layer, a SiO2/Si3N4/SiO2 (ONO) stacked layer and a Si3N4/SiO2 (NO) stacked layer.

12. The trench capacitor of claim 7, wherein said conducting layer includes doped polysilicon.

13. A trench capacitor, comprising:

a substrate having a trench;

a conducting layer filling said trench;

a first capacitor dielectric layer between a surface of said trench and said conducting layer;

a protruding electrode on said substrate around said trench and covering a junction of said trench and said substrate;

a second capacitor dielectric layer between said conducting layer and said substrate, said substrate around said first and second capacitor dielectric layers being a bottom electrode; and

a conducting structure electrically connecting said protruding electrode and said conducting layer, wherein said conducting layer, said protruding electrode, and said conducting structure serve as an upper electrode.

14. The trench capacitor of claim 13, wherein said protruding electrode extends to cover said conducting layer.

15. The trench capacitor of claim 13, wherein said first and second capacitor dielectric layers are at least one of an oxide layer, a SiO2/Si3N4/SiO2 (ONO) stacked layer, and a Si3N4/SiO2 (NO) stacked layer.

16. The trench capacitor of claim 13, wherein said conducting layer and said protruding electrode include doped polysilicon.

17. The trench capacitor of claim 13, wherein said conducting structure is copper (Cu) or tungsten (W).

18. A dynamic random access memory cell, the memory cell comprising:

a substrate having a trench;

a conducting layer filling said trench and extending to said substrate

around said trench;

a capacitor dielectric layer between a surface of said trench and said conducting layer, and between said conducting layer and said substrate, said conducting layer being an upper electrode, and said substrate around said capacitor dielectric layer being a bottom electrode;

a gate electrode on said substrate beside said conducting layer;

a plurality of drain/source regions in said substrate beside two sides of said gate electrode; and

a gate dielectric layer between said gate electrode and said substrate.

19. The dynamic random access memory cell of claim 18, wherein said first and second capacitor dielectric layers is at least one of an oxide layer, a SiO2/Si3N4/SiO2 (ONO) stacked layer, and a Si3N4/SiO2 (NO) stacked layer.

20. The dynamic random access memory cell of claim 18, wherein a material of said capacitor dielectric is the same as a material of said gate dielectric layer.

21. The dynamic random access memory cell of claim 18, wherein a material of said capacitor dielectric is different from a material of said gate dielectric layer.

22. The dynamic random access memory cell of claim 18, wherein said conducting layer and said gate electrode include doped polysilicon.

23. The dynamic random access memory cell of claim 18 further comprising a plurality of spacers on sidewalls of said conducting layer and said gate electrode.

24. The dynamic random access memory cell of claim 23 further comprising a self-aligned silicide layer on surfaces of said conducting layer and said

gate electrode.

25. A dynamic random access memory cell, comprising:

a substrate having a trench;

a conducting layer filling said trench;

a first capacitor dielectric layer between the surface of said trench and said conducting layer;

a protruding electrode on said substrate around said trench and covering a junction of said trench and said substrate;

a second capacitor dielectric layer between said conducting layer and said substrate, said substrate around said first and second capacitor dielectric layers being a bottom electrode;

a gate electrode on said substrate beside said protruding electrode;

a plurality of drain/source regions in said substrate beside two sides of said gate electrode;

a gate dielectric layer between said gate electrode and said substrate; and

a conducting structure electrically connecting said protruding electrode and said conducting layer, and said conducting layer, said protruding electrode, and said conducting structure being an upper electrode.

26. The dynamic random access memory cell of claim 25, wherein said protruding electrode extends to cover said conducting layer.

27. The dynamic random access memory cell of claim 25, wherein said first and second capacitor dielectric layers is at least one of an oxide layer, a SiO2/Si3N4/SiO2 (ONO) stacked layer and a Si3N4/SiO2 (NO) stacked layer.

28. The dynamic random access memory cell of claim 25, wherein said

conducting layer and said protruding electrode include doped polysilicon.

29. The dynamic random access memory cell of claim 25, wherein said conducting structure is copper (Cu) -or tungsten (W).

30. The dynamic random access memory cell of claim 25 further comprising a plurality of spacers on sidewalls of said conducting layer and said gate electrode.

31. The dynamic random access memory cell of claim 30 further comprising a self-aligned silicide layer on surfaces of said conducting layer and said gate electrode.

32. The dynamic random access memory cell of claim 25, wherein a material of said first and second capacitor dielectric layers is the same as a material of said gate dielectric layer.

33. The dynamic random access memory cell of claim 25, wherein a material of said first and second capacitor dielectric layers is different from a material of said gate dielectric layer.